IN THE CLAIMS

Please amend claims 1, 3, 4, 6-9, 11-13, and 15-21, and add new claims 22 and 23, as follows:

1. (Currently Amended) A communication method that is executed by a transmission unit and a reception unit, comprising:

packetizing one or more items of sporadically input data to accompany timing information representing respective input timings of the one or more items of sporadically input data, said timing information being ~~represented by a series of bits, wherein, within a given time interval, a bit value of "1" indicates an input timing for a specific piece of input data;~~ in the form of a plurality of bits, wherein:

each one of said plurality of bits is periodically produced and takes on either a first binary value or a second binary value that is different from the first binary value; and

for each periodically-produced bit, a bit value equal to the first binary value represents a timing at which one of said items of sporadically input data is inputted to the transmission unit, and a bit value equal to the second binary value represents a timing at which no data is inputted to the transmission unit;

transmitting ~~packetized input data accompanying~~ the packetized data along with the timing information from the transmission unit;

receiving the packetized ~~input data accompanying~~ data along with the timing information by the reception unit; and

outputting the packetized [[input]] data as output data at timings based on the timing information from the reception unit, ~~wherein consecutive pieces of said output data are outputted at the same relative timings as the relative input timings of the corresponding input data~~ wherein,

for each bit of the received timing information, when the bit value is equal to the first binary value, a corresponding item of the packetized data is outputted by the reception unit, and when the bit value is equal to the second binary value, no data is outputted by the reception unit, such that respective timings of the output data correspond to said respective input timings of the sporadically input data.

2. (Original) A communication method according to claim 1, wherein the sporadically input data correspond to MIDI data that are produced and input to the transmission unit in a sporadic manner.

3. (Currently amended) A communication method according to claim 1, wherein the transmission unit transmits the packetized ~~input data accompanying~~ data along with the timing information to the reception unit via a network.

4. (Currently Amended) A communication system comprising:

a transmission unit for packetizing one or more items of sporadically input data to accompany timing information representing respective input timings of the one or more items of sporadically input data and for transmitting ~~packetized input data accompanying the timing information, said timing information being represented by a series of bits, wherein, within a given time interval, a bit value of "1" indicates an input timing for a specific piece of input data;~~ the packetized data along with the timing information corresponding thereto, said timing information being in the form of a plurality of bits, wherein:

each one of said plurality of bits is periodically produced and takes on either a first binary value or a second binary value that is different from the first binary value; and

for each periodically-produced bit, a bit value equal to the first binary value represents a timing at which one of said items of sporadically input data is inputted to the transmission unit, and a bit value equal to the second binary value represents a timing at which no data is inputted to the transmission unit; and

a reception unit for receiving the packetized ~~input-data-accompanying~~ data along with the timing information from the transmission unit,

wherein said reception unit outputs the packetized [[input]] data as output data at timings based on the timing information such that ~~consecutive pieces of said output data are outputted at the same relative timings as the relative input timings of the corresponding input data~~, for each bit of the received timing information, when the bit value is equal to the first binary value, a corresponding item of the packetized data is outputted by the reception unit, and when the bit value is equal to the second binary value, no data is outputted by the reception unit, and respective timings of the output data correspond to said respective input timings of the sporadically input data.

5. (Original) A communication system according to claim 4, wherein the sporadically input data correspond to MIDI data that are produced and input to the transmission unit in a sporadic manner.

6. (Currently amended) A communication system according to claim 4, wherein the transmission unit transmits the packetized ~~input-data-accompanying~~ data along with the timing information to the reception unit via a network.

7. (Currently Amended) A transmission unit for use in a communication system performing packet communications, comprising:

an input device for ~~inputting sporadically input~~ sporadically inputting data;

a buffer memory for accumulating the sporadically input data, wherein the buffer memory is periodically initialized ~~every prescribed time~~;

a timing data register for storing timing ~~data representing respective input timings of consecutive pieces of the sporadically input data, said timing data being represented by a series of bits, wherein, within a given time interval, a bit value of "1" indicates an input timing for a specific piece of input~~ data, said timing data being in the form of a plurality of bits, wherein:

each one of said plurality of bits is periodically produced and takes on either a first binary value or a second binary value that is different from the first binary value; and

for each periodically-produced bit, when an item of said sporadically input data is inputted to the buffer memory, the timing data register stores the first binary value for said periodically-produced bit as a representation of the input timing of said item of sporadically input data, and when no item of data is inputted to the buffer memory, the timing data register stores the second binary value for said periodically-produced bit; and

a controller for periodically checking ~~stored content of the timing data register at every prescribed time, wherein the controller performs packetizing of the sporadically input data stored in the buffer memory and the packetized input data accompanying the timing data read from the timing data register are subjected to transmission~~ the timing data stored in the timing data register such that, when, for a given time interval, the bit value corresponding to one of the plurality of bits of the stored timing data is equal to the first binary value, the sporadically input data stored in the buffer memory are packetized and subjected to transmission along with the timing data in said time interval.

8. (Currently amended) The transmission unit according to claim 7, wherein the ~~prescribed time~~ given time interval corresponds to a packet timing that occurs by a prescribed number of shift timings ~~corresponding to said bits of the timing data respectively~~ in correspondence with the plurality of bits forming the timing data.

9. (Currently amended) The transmission unit according to claim 7, wherein the timing data register is a shift register for storing said plurality of bits of the timing data ~~having a prescribed number of bits at every prescribed time corresponding to a packet timing~~.

10. (Original) The transmission unit according to claim 7, wherein the sporadically input data correspond to MIDI data that are produced and input in a sporadic manner.

11. (Currently amended) The transmission unit according to claim 7, wherein the packetized ~~input data accompanying the timing~~ data are subjected to transmission along with the timing data via a network.

12. (Currently Amended) A reception unit for use in a communication system performing packet communications, comprising:

~~a receiver for receiving packetized input data corresponding to sporadically input data from a transmission unit together with timing data representing respective input timings of the input data, said timing data being represented by a series of bits, wherein, within a given time interval, a bit value of "1" indicates an input timing for a specific piece of input data~~ a receiver for receiving, from a transmission unit, packetized data accompanied by timing data corresponding thereto, said packetized data including one or more items of data sporadically inputted into said transmission unit and said timing data being in the form of a plurality of bits, wherein:

each one of said plurality of bits is periodically produced and takes on either a first binary value or a second binary value that is different from the first binary value; and

for each periodically-produced bit, a bit value equal to the first binary value represents a timing at which one of said items of the sporadically input data is inputted to the transmission unit, and a bit value equal to the second binary value represents a timing at which no data is inputted into the transmission unit;

a buffer memory for accumulating the packetized [[input]] data received by the receiver;

a timing data register for storing the timing data received by the receiver; and

~~a controller for outputting, as output data, the packetized input data read from the buffer memory at timings based on the timing data such that consecutive pieces of said output data are outputted at the same relative timings as the relative input timings of the corresponding input data~~ a controller for periodically processing the timing data such that, for each bit of the timing data, when the bit value of the timing data is equal to said first binary value, the item of packetized data corresponding thereto is read from the buffer memory and outputted, and when the bit value of the timing data is equal to said second binary value, no data is read from the buffer memory.

13. (Currently amended) The reception unit according to claim 12, wherein the timing data register is a shift register for storing said plurality of bits of the timing data ~~having a prescribed number of bits at every prescribed time corresponding to a packet timing~~.

14. (Original) The reception unit according to claim 12, wherein the sporadically input data correspond to MIDI data that are produced and input to the transmission unit in a sporadic manner.

15. (Currently amended) The reception unit according to claim 12, wherein the receiver receives from the transmission unit the packetized ~~input-data-accompanying~~ data along with the timing data via a network.

16. (Currently Amended) A computer-readable recording medium storing a communication program which when executed causes a computer to perform a transmission method for use in a communication system performing packet communications, said transmission method comprising:

~~inputting sporadically input~~ sporadically inputting data;

accumulating the sporadically input data in a buffer memory that is periodically initialized ~~every prescribed time~~;

storing timing data representing respective input timings of ~~consecutive pieces~~ one or more items of the sporadically input data by a timing data register, said timing data being ~~represented by a series of bits, wherein, within a given time interval, a bit value of "1" indicates an input timing for a specific piece of input data~~ in the form of a plurality of bits, wherein:

each one of said plurality of bits is periodically produced and takes on either a first binary value or a second binary value that is different from the first binary value; and

for each periodically-produced bit, when an item of said sporadically input data is inputted to the buffer memory, the timing data register stores the first binary value for said periodically-produced bit as a representation of the input timing of said item of sporadically input data, and when no item of data is inputted to the buffer memory, the timing data register stores the second binary value for said periodically-produced bit;

periodically checking ~~stored content of the timing data register at every prescribed time~~ the timing data stored in the timing data register and, when, for a given time interval, the bit

value corresponding to one of the plurality of bits of the stored timing data is equal to the first binary value, packetizing the sporadically input data stored in the buffer memory; and

~~packetizing the sporadically input data stored in the buffer memory; and~~

transmitting the packetized ~~input data accompanying the timing data read from the timing data register~~ data along with the timing data in said time interval.

17. (Currently amended) The computer-readable recording medium according to claim 16, wherein the sporadically input data correspond to MIDI data that are produced and input in a sporadic manner.

18. (Currently amended) The computer-readable recording medium according to claim 16, wherein the packetized ~~input data accompanying the timing~~ data are subjected to transmission along with the timing data via a network.

19. (Currently Amended) A computer-readable recording medium storing a communication program which when executed causes a computer to perform a reception method for use in a communication system performing packet communications, said reception method comprising:

~~receiving packetized input data corresponding to sporadically input data from a transmission unit together with timing data representing respective input timings of the input data, said timing data being represented by a series of bits, wherein, within a given time interval, a bit value of "1" indicates an input timing for a specific piece of input data~~ receiving, from a transmission unit, packetized data accompanied by timing data corresponding thereto, said packetized data including one or more items of data sporadically inputted into said transmission unit and said timing data being in the form of a plurality of bits, wherein:

each one of said plurality of bits is periodically produced and takes on either a first binary value or a second binary value that is different from the first binary value; and

for each periodically-produced bit, a bit value equal to the first binary value represents a timing at which one of said items of the sporadically input data is inputted to the transmission unit, and a bit value equal to the second binary value represents a timing at which no data is inputted into the transmission unit;

accumulating the received packetized [[input]] data by a buffer memory;

storing the received timing data in a timing data register; and

outputting, as output data, the packetized ~~input data read from the buffer memory at timings based on the timing data such that consecutive pieces of said output data are outputted at the same relative timings as the relative input timings of the corresponding input~~ data such that, for each bit of the timing data, when the bit value of the timing data is equal to said first binary value, the item of packetized data corresponding thereto is read from the buffer memory and outputted, and when the bit value of the timing data is equal to said second binary value, no data is read from the buffer memory.

20. (Currently amended) The computer-readable recording medium according to claim 19, wherein the sporadically input data correspond to MIDI data that are produced and input in a sporadic manner.

21. (Currently amended) The computer-readable recording medium according to claim 19, wherein the packetized ~~input data accompanying the timing~~ data are received along with the timing data via a network.

22. (New) The transmission unit according to claim 7, wherein the first binary value is "1" and the second binary value is "0".

23. (New) The reception unit according to claim 12, wherein the first binary value is "1" and the second binary value is "0".